# AND8002/D

# Clock Generation and Clock and Data Marking and Ordering Information Guide

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APPLICATION NOTE

## Introduction

This application note describes the device markings and ordering information for the following ON Semiconductor families (refer to the respective family data book for family information):

- ECLinPS Lite™
- ECLinPS MAX™
- ECLinPS Plus™
- ECLinPS™
- GigaComm™
- Low Voltage ECLinPS Plus™
- Low Voltage ECLinPS Lite™
- Low Voltage ECLinPS™
- PureEdge™

Note that data sheet information takes precedence over this application note if there are any differences.

## Application Note Information

This application note is divided into the following sections:

- Section 1: Data Sheet Marking Diagrams – The diagrams provide identification, traceability, date, and packaging information.
- Section 2: Data Sheet Ordering Information Tables – The tables list the device order numbers for every available device configuration.

## SECTION 1: Data Sheet Marking Diagrams

### Device Marking Examples

The marking format is dependent upon the device package, and larger device packages allow the inclusion of more information on the face of the device. On the larger packages where marking space permits, the Pb Free designator will be an additional suffix letter G added to the traceability and date code line. A marking example for the large 52−pin NB100LVEP222 is shown below. Note that the device marking includes the following coded information that is described in later sections:

- Code 1. Circuit Identification Code
- Code 2. Temperature Compensation Code
- Code 3. Family Identification Code
- Code 4. Function Type Code
- Code 5. Assembly Location Traceability Code
- Code 6. Wafer Lot Traceability Code
- Code 7. Year Date Code
- Code 8. Work Week Date Code
- Code 9. Pb Free Designator

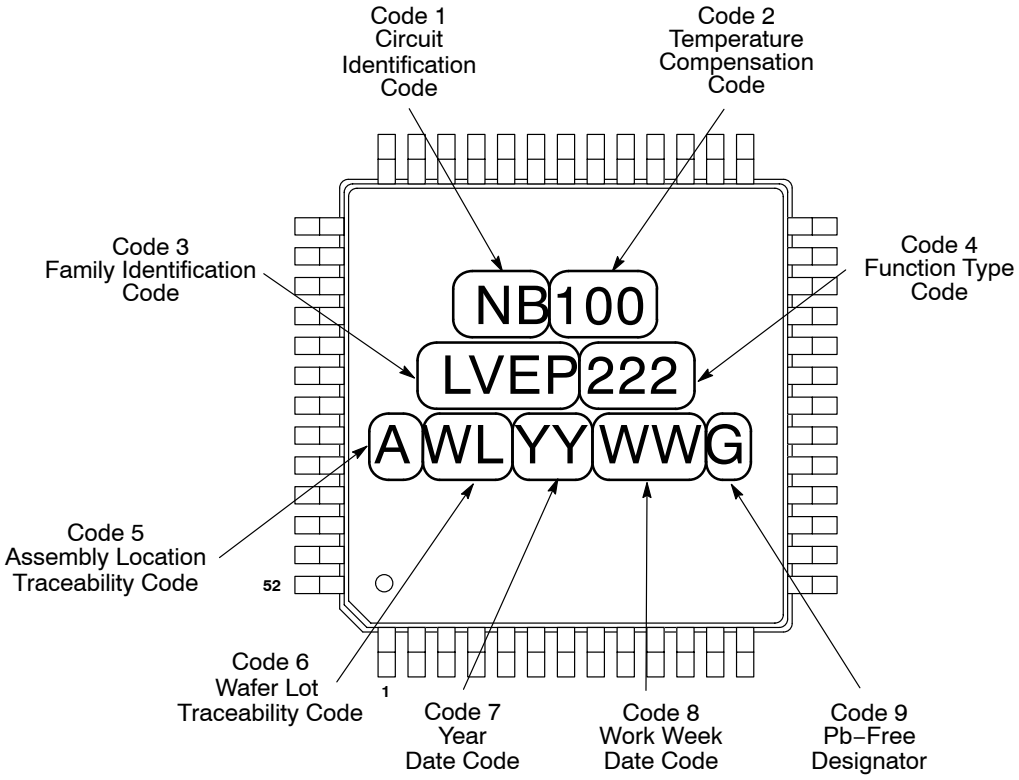



**Figure 1. 52−Pin Marking Example**

A marking example for the 8−pin TSSOP MC100EP16 device is shown in Figure 2. Note that the 8−pin package does not allow for as much marking information as the 52−pin package. On the smaller package where marking space is limited, the Pb Free designator will be an additional ”Dot” centered below the traceability and date code line, or else a ”Microdot” positioned below the right side of the traceability and date code line.

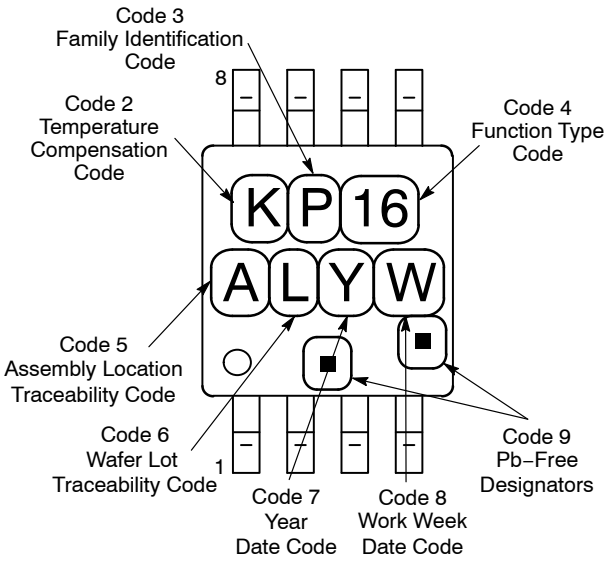



**Figure 2. 8−Pin Marking Example**

**Code 1. Circuit Identification Code**

MC identifies Motorola Circuits that are now owned by ON Semiconductor. NB identifies circuits that were introduced by ON Semiconductor. XC (X on 8−pin packages) identifies Preproduction/Prereliability devices, and PC (P on 8−pin packages) identifies Prototype devices. Contact ON Semiconductor for further information on non−released device markings.

**Code 2. Temperature Compensation Code**

There are two Temperature Compensation codes. The “10” code indicates that the device characteristics are temperature dependent (refer to AND8066/D for additional information). The “100” identification code indicates that the device characteristics are not temperature dependent.

**Code 3. Family Identification Code**

Family Identification Codes are shown in the following table.

**Table 1. FAMILY IDENTIFICATION CODES**

| Family | TSSOP − 8 Code 3 | SO − 8 Code 3 | Over 8 − Pin Code 3 |
|---|---|---|---|
| ECLinPS Lite | L | EL | EL |
| ECLinPS MAX | 6L | 6L | 6L |
| ECLinPS Plus | P | EP | EP |
| ECLinPS | | | E |
| GigaComm | | | SG, 7 |
| Low Voltage ECLinPS Plus | U | VP | LVEP |
| Low Voltage ECLinPS Lite | V | VL | LVEL |
| Low Voltage ECLinPS | | | LVE |
| PureEdge | | | X, V, T |
| ECLinPS Lite Translator | T | LT | ELT |
| ECLinPS Plus Translator | A | PT | EPT |
| Low Voltage ECLinPS Lite Translator | R | VT | LVELT |

**Code 4. Function Type Code**

Each device is assigned a unique function type identifier.

**Code 5. Assembly Location Traceability Code**

The one character Assembly Location Traceability Codes identify the final assembly location and are shown in the following table.

**Table 2. ASSEMBLY LOCATION TRACEABILITY CODES**

| Code 5 | Assembly Site | Location |
|---|---|---|
| 5 | UNISEM International LTD | Batam Island, Indonesia |
| L | Amkor Technology Philippines | Manila, Philippines |
| 9 | ASAT Holdings Limited | New Territories, Hong Kong |
| G | UTAC Thai LTD | Bangkok, Thailand |
| C | ASE (Korea) Inc. | Seoul, Korea |
| P | ON Semiconductor Carmona | Carmona, Philippines |
| R | ON Semiconductor Sbn | Seremban, Malaysia |
| D1 | ASE – Chung Li (METL) | Chung – Li, Taiwan |

### Code 6: Wafer Lot Traceability Code

The use of a one or two character Wafer Lot Traceability Code is dependent upon the package size and is shown in Table 3. The Wafer Lot Traceability Code in conjunction with the Work Week Date Code provides unique wafer lot identification.

### Code 7. Year Date Code

The use of a one or two character Year Date Code is dependent upon the package size and as shown in Table 3.

### Code 8. Work Week Date Code

The use of a one or two character Work Week Date Code is dependent upon the package size and is listed in Table 3.

### Traceability and Date Code Tables

The coding and an example for each available package type is shown in Table 3. Note that the smaller packages use a one−character alpha code for the “Year”, and a one−character alpha code for the “Work Week”. The alpha codes are deciphered in Table 4.

**Table 3. TRACEABILITY AND DATE CODE MARKINGS AND EXAMPLES**

| Package | Traceability Codes | | Date Codes | |
|---|---|---|---|---|
| | Assembly Code (Code 5) | Wafer Lot (Code 6) | Year (Code 7) | Work Week (Code 8) |
| **CDIP−16** | A | WL | YY | WW |
| Example | 5<br>ATP1 | AA<br>First Lot | 96<br>1996 | 46<br>46th Week |
| **EIAJ SO−14** | A | L | Y | W |
| Example | X<br>ASE CL | B<br>Second Lot | B<br>End 2002 | T<br>46th Week |
| **FCBGA−16** | A | L | Y | W |
| Example | K<br>ASE K | A<br>First Lot | B<br>End 2002 | T<br>46th Week |
| **LQFP−32, LQFP−52, LQFP−64** | A | WL | YY | WW |
| Example | X<br>ASE CL | AA<br>First Lot | 96<br>1996 | 46<br>46th Week |
| **PLCC−20, PLCC−28** | A | WL | YY | WW |
| Example | P<br>OSPI | AA<br>First Lot | 96<br>1996 | 46<br>46th Week |
| **QFN−10, QFN−16, QFN−24** | A | L | Y | W |
| Example | 9<br>ASAT | B<br>Second Lot | B<br>End 2002 | T<br>46th Week |
| **SO−8** | A | L | Y | W |
| Example | X<br>ASE CL | B<br>Second Lot | B<br>End 2002 | T<br>46th Week |
| **SO−16** | A | WL | Y | WW |
| Example | X<br>ASE CL | AA<br>First Lot | B<br>End 2002 | 46<br>46th Week |
| **SO−20** | A | WL | YY | WW |
| Example | 2<br>AIT | AA<br>First Lot | 96<br>1996 | 46<br>46th Week |
| **TSSOP−8, TSSOP−16, TSSOP−20** | A | L | Y | W |
| Example | 5<br>ATP1 | B<br>Second Lot | B<br>End 2002 | T<br>46th Week |

**Table 4. ALPHA YEAR AND WORK WEEK DATE CODES**

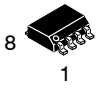
| Alpha Year Date Codes (Code 7) | | | Alpha Work Week Date Codes (Code 8) | |
|---|---|---|---|---|
| Year | First or Second Half−Year | | First Half−Year Work Week | Second Half−Year Work Week |
| A = 2002 | First Half | | A = 01 | A = 27 |
| B = 2002 | Second Half | | B = 02 | B = 28 |
| C = 2003 | First Half | | C = 03 | C = 29 |
| D = 2003 | Second Half | | D = 04 | D = 30 |
| E = 2004 | First Half | | E = 05 | E = 31 |
| F = 2004 | Second Half | | F = 06 | F = 32 |
| G = 2005 | First Half | | G = 07 | G = 33 |
| H = 2005 | Second Half | | H = 08 | H = 34 |
| I = 2006 | First Half | | I = 09 | I = 35 |
| J = 2006 | Second Half | | J = 10 | J = 36 |
| K = 2007 | First Half | | K = 11 | K = 37 |
| L = 2007 | Second Half | | L = 12 | L = 38 |
| M = 2008 | First Half | | M = 13 | M = 39 |
| N = 2008 | Second Half | | N = 14 | N = 40 |
| P = 2009 | First Half | | O = 15 | O = 41 |
| R = 2009 | Second Half | | P = 16 | P = 42 |
| S = 2010 | First Half | | Q = 17 | Q = 43 |
| T = 2010 | Second Half | | R = 18 | R = 44 |
| U = 2011 | First Half | | S = 19 | S = 45 |
| V = 2011 | Second Half | | T = 20 | T = 46 |
| W = 2012 | First Half | | U = 21 | U = 47 |
| X = 2012 | Second Half | | V = 22 | V = 48 |
| Y = 2013 | First Half | | W = 23 | W = 49 |
| Z = 2013 | Second Half | | X = 24 | X = 50 |
| | | | Y = 25 | Y = 51 |
| | | | Z = 26 | Z = 52 |

## Package Information

The marking diagram includes the following package information:

- Package: The industry standard designation for the package.
- Package Suffix: This suffix is used to order the device, and is part of the device order number listed in the Ordering Information table. Refer to the following "Ordering Information" section.
- Package Case Number: The industry standard case designation for the package.

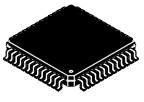
Packaging information examples from the MC100EP16 and NB100LVEP222 data sheets are shown below.




**SO−8**
**D SUFFIX**
**CASE 751**


**TSSOP−8**
**DT SUFFIX**
**CASE 948R**

**Figure 3. 8−Pin Packaging Information Example**



**52−LEAD LQFP**
**THERMALLY ENHANCED**
**CASE 848H**
**FA SUFFIX**

**Figure 4. 52−Pin Packaging Information Example**

## SECTION 2: Data Sheet Ordering Information Tables

### Ordering Information Examples

Ordering Information tables from the MC100EP16, NB100LVEP222, and NBSG16 data sheets are shown below.

**Table 5. ORDERING INFORMATION TABLE EXAMPLES**

| Data Sheet | Ordering Information Table | | |
|---|---|---|---|
| | Device | Package | Shipping |
| MC10/100EP16 | MC10EP16D | SO−8 | 98 Units/Rail |
| | MC10EP16DR2 | SO−8 | 2500 Tape & Reel |
| | MC100EP16D | SO−8 | 98 Units/Rail |
| | MC100EP16DR2 | SO−8 | 2500 Tape & Reel |
| | MC10EP16DT | TSSOP−8 | 100 Units/Rail |
| | MC10EP16DTR2 | TSSOP−8 | 2500 Tape & Reel |
| | MC100EP16DT | TSSOP−8 | 100 Units/Rail |
| | MC100EP16DTR2 | TSSOP−8 | 2500 Tape & Reel |
| NB100LVEP222 | NB100LVEP222FA | LQFP−52 | 160 Units/Tray |
| | NB100LVEP222FAR2 | LQFP−52 | 1500 Tape & Reel |
| NBSG16 | NBSG16BA | 4x4 mm FCBGA−16 | 810 Units/Rail |
| | NBSG16BAR2 | 4x4 mm FCBGA−16 | 2500 Tape & Reel |
| | NBSG16BA100 | 4x4 mm FCBGA−16 | 100 Units/Tray |
| | NBSG16BA500R2 | 4x4 mm FCBGA−16 | 500 Tape & Reel |

The following table decodes the device order numbers for some of the above examples. Note that the order number is made up of the Codes from the data sheet Marking Diagram. Refer to the previous “Code” sections for a description of the codes.

**Table 6. DEVICE ORDER NUMBER DECODING**

| Device Order Number | Circuit Identification Code (Code 1) | Temperature Compensation Code (Code 2) | Family Identification Code (Code 3) | Function Type Code (Code 4) | Package Suffix |
|---|---|---|---|---|---|
| MC100EP16DT | MC<br>Motorola Circuit | 100 | EP<br>ECLinPS Plus | 16<br>Unique Identifier | DT<br>TSSOP−20 |
| NB100LVEP222FA | NB<br>ON Circuit | 100 | LVEP<br>Low Voltage EP | 222<br>Unique Identifier | FA<br>LQFP−52 |
| NBSG16BA | NB<br>ON Circuit | N/A | SG<br>GigaComm | 16<br>Unique Identifier | BA<br>FCBGA−16 |

### Package Suffix

The package suffixes are shown in the data sheet Marking Diagram.

**Table 7. ECLinPS AND GigaComm PACKAGE SUFFIXES**

| Suffix | Package | Pins | Case | Description |
|---|---|---|---|---|
| BA | FCBGA−16 | 16 | 489 | Ball Grid Array |
| D | SO−16 | 16 | 751B | Small Outline IC |
| D | SO−8 | 8 | 751 | Small Outline IC |
| D | SO−14 | 14 | | Small Outline IC |
| DT | TSSOP−16 | 16 | 948F | Thin Shrink Small Outline Package |
| DT | TSSOP−20 | 20 | 948E | Thin Shrink Small Outline Package |
| DT | TSSOP−28 | 28 | 948A | Thin Shrink Small Outline Package |
| DT | TSSOP−8 | 8 | 948R | Thin Shrink Small Outline Package |
| DW | SO−20 | 20 | 751D | Small Outline IC |
| FA | LQFP−32 | 32 | 873A | Leaded Quad Flat Pack |
| FA | LQFP−52 | 52 | 848−D | Leaded Quad Flat Pack |
| FA | LQFP−52 | 52 | 848H | Leaded Quad Flat Pack |
| FA | LQFP−64 | 64 | 848G | Leaded Quad Flat Pack |
| FN | PLCC−20 | 20 | 775 | Plastic Leaded Chip Carrier |
| FN | PLCC−28 | 28 | 776 | Plastic Leaded Chip Carrier |
| L | CDIP−16 | 16 | 620 | Ceramic DIP |
| LN | CLCC−6 | 6 | 848AB | Ceramic Leadless Chip Carrier 6.5 x 7 mm |
| M | Micro−10 | 10 | 846B | Micro−10 |
| M | EIAJ SO−14 | 14 | 965 | EIAJ Small Outline IC |
| M | EIAJ SO−16 | 16 | 966 | EIAJ Small Outline IC |
| MN | DFN8 | 8 | 506AA | Dual Flat No−Lead |
| MN | QFN−16 | 16 | 485G | Quad Flat No − Lead |
| MN | QFN−24 | 24 | 485L | Quad Flat No − Lead |
| MN | QFN−52 | 52 | 485M | Quad Flat No − Lead |
| P | PDIP−16 | 16 | 648 | Plastic DIP |
| P | PDIP−24 | 24 | 724 | Plastic DIP |

### Shipping Specification

The “Shipping” column in the Ordering Information table specifies the shipping configuration that corresponds to the device order number. Add R2 to the regular package suffix to order tape and reel shipping configurations. Refer to Brochure BRD8011/D for further tape and reel information.

### For Additional Information

Additional traceability and date code information is available upon request. To make a request, please visit our website at http://www.onsemi.com and click on “Technical Support,” or contact the Technical Information Center (TIC) at 1−800−282−9855.

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